# COMPACT INTEGRATED COPLANAR T/R-MODULES FOR AUTOMOTIVE APPLICATIONS

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***Abstract*** **- Integrated transmit and receive MMICs for automotive applications have been realized in coplanar waveguide technology, using a 0.15 µm PHEMT process. The transmitter chip delivers an output power of 10 dBm at the antenna and the LO-ports. The receiver has an overall conversion gain of 10 dB for an LO-power of -10 dBm. Both chips only require an area of 3x2 mm². For an improved higher power version of the transmitter, a new nonlinear HEMT-model has been used for the design of a power amplifier, resulting in excellent agreement between predicted and measured output performance at 76 GHz.**

## I. INTRODUCTION

W-band radar systems for automotive applications have focused the interest on compact and inexpensive integrated circuits on GaAs. Very compact multifunction MMICs for W-band applications can be realized in coplanar technology, allowing a cost reduction in chip processing and in inter-chip connections. In previous work [1, 2], it has been demonstrated that amplifiers and VCOs based on coplanar technology achieve a performance comparable to those based on microstrip technology [3].

MMICs for FMCW systems require multiple active and passive circuits like oscillators, high gain and medium power amplifiers, mixers, and various couplers. For design verification of more complex chips, all crucial circuits were additionally realized as 2-port chips. Depending on the system specifications, bond wires of significant length, compared to the wavelength at the operating frequency, have to be accounted for on the chip design [4].

For a collision avoidance radar system at 76 GHz, an integrated transmitter and an integrated receiver front-end were developed and fabricated with our PHEMT process on 3" s.i. GaAs wafers. The T-shaped gates have a length of 0.15 µm, defined by e-beam lithography using a three-level photoresist

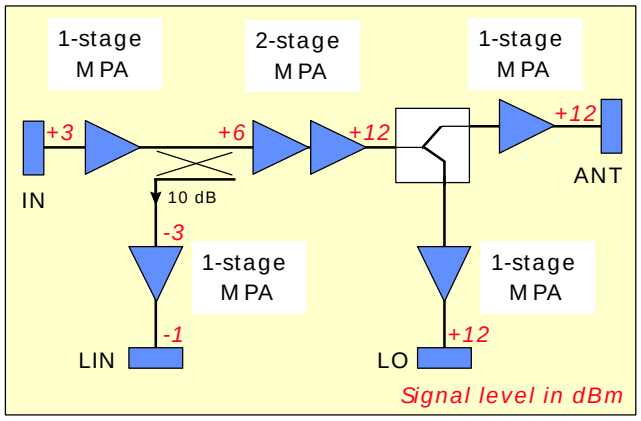


**Fig. 1:** Block diagram of integrated 76 GHz transmitter MMIC.

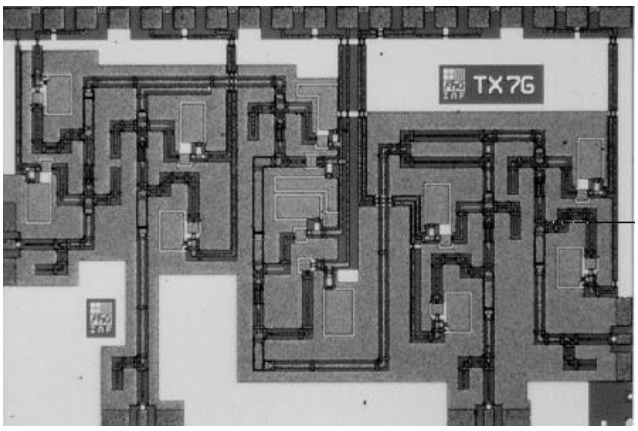


**Fig. 2:** Chip photograph of coplanar transmitter MMIC (3x2 mm²).

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technology. In common-source configuration, the devices have an extrinsic peak transconductance of 800 mS/mm for a gate bias of 0.35 V with a drain current of roughly 240 mA/mm. Biased for maximum gain, single gate devices achieve an $f_T$ and $f_{max}$ of 115 and 160 GHz, respectively. The maximum drain current is 640 mA/mm. A 2x60 µm device offers an MAG of 6.5 dB at 76 GHz.

## II. TRANSMIT MMIC

A block diagram of the integrated transmitter is depicted in Fig. 1. A total of 6 medium power amplifiers serve to deliver power from a coplanar VCO [2] to the antenna (ANT), to the LO-port of the receiver (LO), and to an oscillator control loop (LIN). A minimum RF-power of 10 mW has to be available at both the transmitter antenna port and the LO-port of the receiver. The power is split in two parts by means of a Wilkinson divider [5]. Via a 10 dB coplanar coupled-line directional coupler, a small fraction of the input signal is fed to a linearizer loop for the frequency modulation of the RF-source. The measured output power at both the antenna- and LO-ports is 10 dBm, for an input power of 3 dBm, as can be seen in Fig. 3, and saturates at 11 dBm for an input power of 6 dBm. The dissipated DC-power is 0.4 W. The chip, shown in the photograph of Fig. 2, requires an area of only 3x2mm².

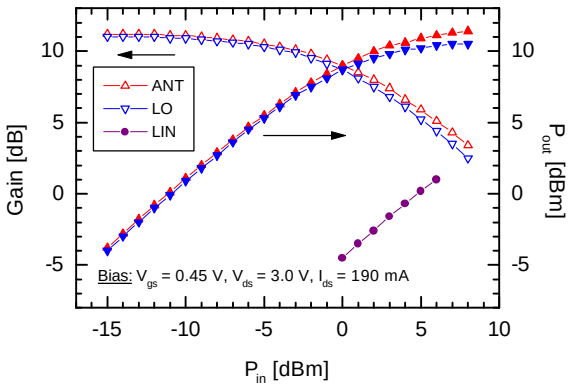


**Fig. 3:** Output power of transmitter MMIC at the three output ports vs. input power.

As part of an improved transmit MMIC with higher output power, we designed a 2-stage MPA on the basis of our analytical nonlinear HEMT-model, having a 4x45 µm FET in the first and a 4x60 µm FET in the second stage. The model consists of five bias dependent elements: the three current sources $I_{gs}$, $I_{gd}$, $I_{ds}$ and the two charge sources $Q_{gs}$ and $Q_{gd}$, which are based on the gate charge $Q_g$. For the gate-source current source, the well-known diode equation

$$I_{gs} = I_{gs0} \cdot \left( \exp\left( \frac{qV_{gsi}}{\eta kT} \right) - 1 \right) \tag{1}$$

is used, with $I_{gs0}$ being the saturation current, $\eta$ being the ideality factor and $V_{gsi}$ being the intrinsic gate-source voltage. The breakdown characteristic of the gate-drain diode is modeled by the sum of two diode equations with different $I_0$ and $\eta$. The drain current is described by the product of three terms,

$$I_{ds} = f_1(V_{gsi}) \cdot f_2(V_{gsi}, V_{dsi}) \cdot f_3(V_{dsi}) \tag{2}$$

with $V_{gsi}$ and $V_{dsi}$ being the intrinsic nodal voltages. As developed in [6], the functions $f_1$, $f_2$, $f_3$ are defined as

$$f_1(V_{gsi}) = CD_{VSB}\left[1 + \tanh\left(\delta \cdot (V_{gsi} - V_{SB})\right)\right] + CD_{VC}\left[1 + \tanh\left(\beta \cdot (V_{gsi} - V_C) + \gamma \cdot (V_{gsi} - V_C)^3\right)\right]$$

$$f_2(V_{gsi}, V_{dsi}) = 1 + \frac{\lambda}{1 + \Delta\lambda \cdot (V_{gsi} - V_{to})} V_{dsi} \tag{4}$$

$$\text{with} \quad V_{to} = V_c - \frac{2}{\beta}$$

$$f_3(V_{dsi}) = \tanh(\alpha \cdot V_{dsi}) \tag{5}$$

The capacitances $C_{gs}$ and $C_{gd}$ represent the derivatives of the gate charge with respect to the intrinsic voltages $V_{gsi}$ and $V_{gdi}$, respectively. For the gate charge, the following empirical expression was found:

$$Q_g(V_{gsi}, V_{dsi}) = A \cdot [fq_1 \cdot fq_2] + E \cdot [V_{gsi} - 0.5 \cdot V_{dsi}] \tag{6}$$

where

$$fq_1(V_{gsi}, V_{dsi}) = \frac{1}{B} \cdot \ln\left[\cosh(B \cdot w)\right] + w \tag{7}$$

$$\text{with } w(V_{gsi}, V_{dsi}) = (V_{gsi} - V_1) - \frac{0.5}{C} \cdot \tanh(C \cdot V_{dsi})$$

$$fq_2(V_{dsi}) = D \cdot \ln\left[\cosh(F \cdot V_{dsi})\right] + 1 \tag{8}$$

$Q_g$ fulfills the condition of charge conservation, which means that the charge $Q_g$ can be determined from the contour integration of the capacitances independently of the path.

The parasitics were extracted for 2- and 4-finger devices. The parameters for the nonlinear kernel, modeling only the active zone of the FET, are derived from a 2x60 µm device and assumed to be equal for all device geometries. The simulated S-parameters were compared with measured data up to 120 GHz both for different bias points and for devices of different gate width.

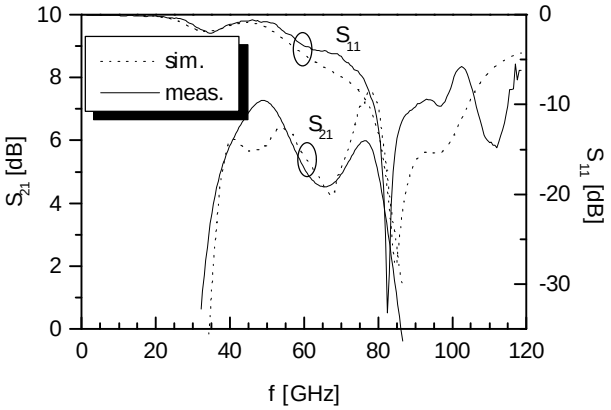


**Fig. 4:** Measured and simulated S-parameters of improved MPA from 0-120 GHz.

Using our CPW-library [7] and the nonlinear HEMT-model, the simulated and measured S-parameters of this 2-stage amplifier are in excellent agreement, as can be seen in Fig. 4. The measured and simulated output performance of this amplifier is shown in Fig. 5. The large-signal behavior of this MPA was precisely predicted by means of a harmonic balance simulation, resulting in a calculated and measured $P_{-1\,dB}$ of 11 dBm and a saturation power of more than 15 dBm at 76.5 GHz. To our knowledge,

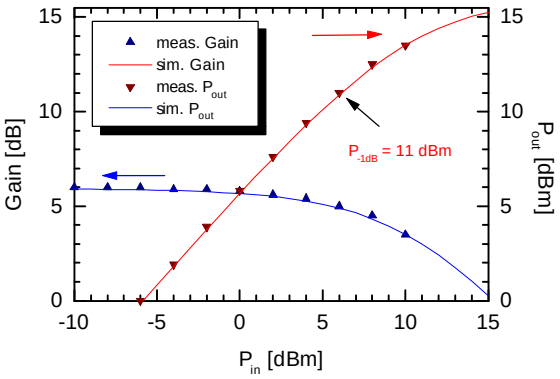


**Fig. 5:** Measured and simulated output power vs. input power of improved MPA at 76 GHz.

this is the first comparison between measured and simulated large-signal behavior at W-band frequencies.

## III. Receive MMIC

The integrated receiver front-end, as illustrated in the block diagram of Fig. 6, incorporates a 4-stage LNA in the RF path, a balanced diode mixer, and a 2-stage LNA cascaded with a 2-stage MPA in the LO path. The gain in the RF path and in the LO path are 18 dB and 16 dB, respectively. Fig. 7 also shows the chip, which has a size of only 3 x 2 mm². For the diode mixer, an area saving reduced-size branch-line coupler with capacitively loaded λ/8-lines is used to balance the LO- and RF-signals at the two diodes. Coplanar branch-line couplers were theoretically and experimentally investigated by means of 2-port test

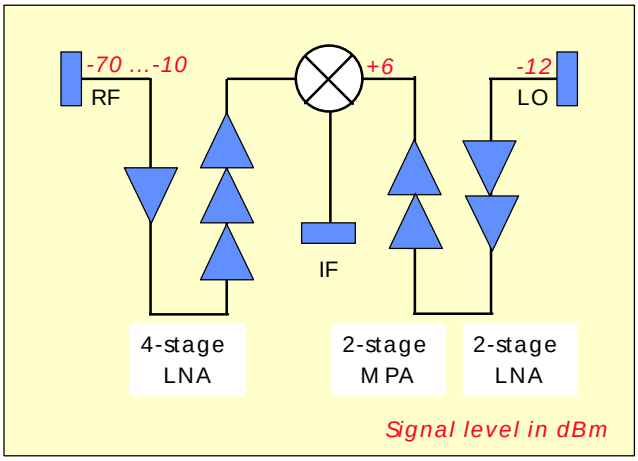


**Fig. 6:** Block diagram of integrated 76GHz receiver MMIC.

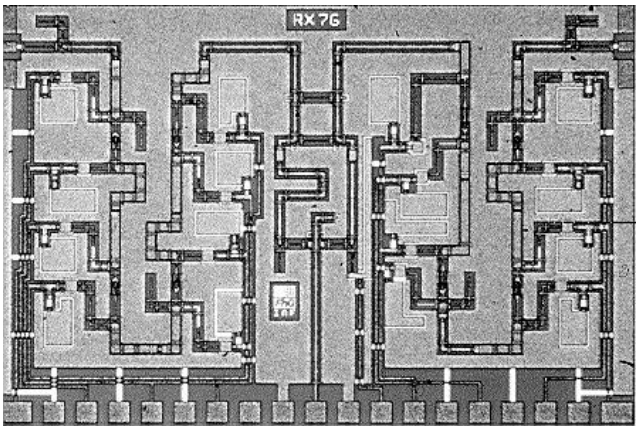


**Fig. 7:** Chip photograph of coplanar receiver MMIC (3x2 mm²).

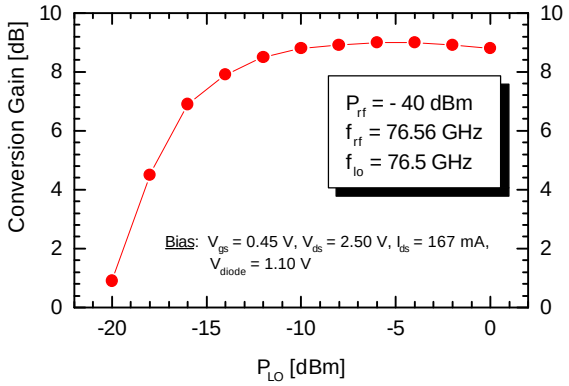


**Fig. 8:** Measured conversion loss of front-end MMIC vs. LO-power.

structures [8]. The diodes are realized as HEMT-diodes. The conversion loss and the DSB noise figure of the mixer are 10 dB and 11 dB, respectively, for an LO-power of 8 dBm. The LO-to-RF-isolation is better than 16 dB. As can be seen in Fig. 8, the overall conversion gain of the front-end is 9 dB for an LO-power of -10 dBm at 76.56 GHz and an RF-power of -40 dBm at 76.5 GHz. The total DC-power consumption is 0.4W.

## IV. Conclusion

Compact transmit and receive MMICs in coplanar technology were designed and fabricated, for use in automotive radars at 77 GHz. For the improvement of the transmitted power, a new 2-stage amplifier was designed by means of an analytical nonlinear model, achieving good agreement between measured and simulated large signal performance at W-band frequencies. The chips were tested in a prototype system, which achieved the required performance [9]. The reproducible realization of amplifiers, oscillators, and mixers with a single technology reveals the chance to further increase the integration level and thus reduce the system costs of an RF front-end. The approach in coplanar waveguide technology results in chips of small size and therefore offers an enormous potential to meet the cost target for a high volume production of MMICs for automotive applications.

## V. Acknowledgement

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